EM785830AA

8-BIT MICRO-CONTROLLER

Version 1.6

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Version History

Specification Revision History	
Version	Content
EM785830AA	
1.0	Initial version
1.1	Add 17.9MHz main CLK
1.2	Add code option “ADIS” to determine AD channel
1.3	1. Change “ADIS” define 2. ADD eFHP5830A, eFHP5830AA, and eFHP5830BA package
1.4	1. ADD the description about ADC’s offset voltage
1.5	1. Modify stack level from 16 to 12 2. Modify program ROM size from 4K to 16K 3. Rename “eFH5830A” to eFH5830AA 4. Remove IDLE mode 5. Change AD channel from 8 to 4 6. Remove 17.9MHz main CLK
1.6	1.Rename from eFH5830AA to EM785830AA

Relative to EM785830AA’s ROM-less, OTP and mask:

ROM-less	OTP	Mask
ICE5830	EM78P5830A	EM785830AA
	EM78P5830AA	

Difference between EM785830AA/EM78P5830A/EM78P5830AA

Some differences are between EM78P5830A, EM78P5830AA and EM78P5830BA, these difference are list at next table:

	EM785830AA	EM78P5830A	EM78P5830AA
ADIS (code option)	Un-effect (4 channel only)	Un-effect (4 channel only)	Un-effect (4 channel only)
VERSEL (code option)	Must = 0	Un-effect	Must = 0
PHO (code option)	Must = 0	Un-effect	Must = 0
MS (IOCC page1 bit0)	Must = 1	Must = 1	Un-effect
AD resolution	10 bit	8 bit	10 bit
Stack number	12	16	16

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

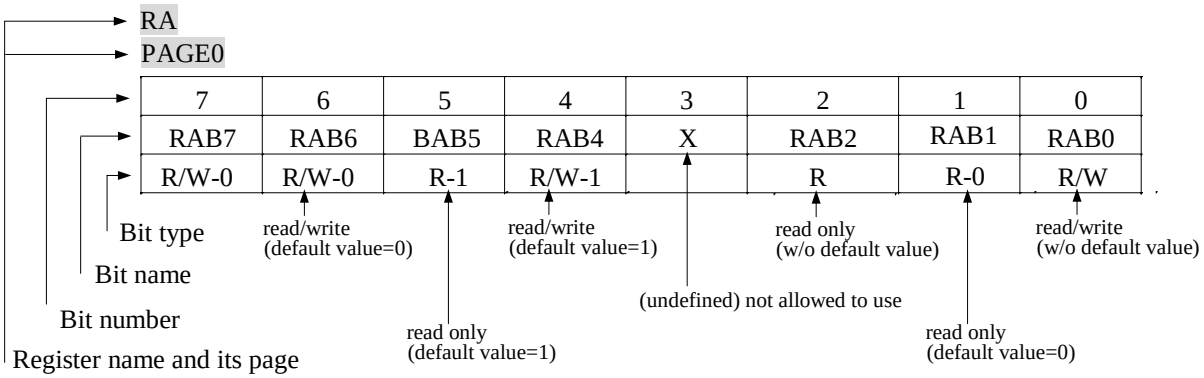
1. There are some undefined bits in the registers. The values in these bits are unpredicted. These bits are not allowed to use. We use the symbol “-” in the spec to recognize them. ***A fixed value must be write in some specific unused bits by software or some unpredicted wrong will occur.***

These bits are as below.

Register			Default value	Initial Setting value (by user software)	Effect
Register	PAGE	Bit			
R7	1	1	0	0	RAM access will error
RA	0	7	0	0	Un-expect error
RA	2	0~7	0	0	Un-expect error
RD	0	0~2	0	0	Power consumption increase
RD	0	4	X	1	Un-expect error

RD	0	5~6	X	0	Un-expect error
RE	0	0~3		0	Un-expect error
IOC5	0	5~7	1	0	Power consumption increase
IOC6	0	0~1	1	0	Power consumption increase
IOC6	1	0~1	0	0	Power consumption increase
IOC7	0	1~2;7	1	0	Power consumption increase
IOC7	1	1~2;7	0	0	Power consumption increase
IOC8	0	0~7	1	0	Power consumption increase
IOC8	1	0~7	0	0	Power consumption increase
IOC9	1	0~7	0	0	Un-expect error
IOCA	1	3,6	0	0	Power consumption increase
IOCB	0	0~7	1	0	Power consumption increase
IOCC	0	0;3~7	1	0	Power consumption increase
IOCC	1	2~7	0	***0***	Un-expect error
IOCE	0	0~3	0	0	Un-expect error
IOCF	0	4~6	0	0	Un-expect error

2. You will see some names for the register bits definitions. Some name will be appear very frequently in the whole spec. The following describes the meaning for the register's definitions such as bit type, bit name, bit number and so on.



3. *Always set IOCC PAGE1 bit 0 = 1 otherwise partial ADC function cannot be used.*

4. *Please do not switch MCU operation mode from normal mode to sleep mode directly. Before into sleep mode, please switch MCU to green mode.*

5. *While switching main clock (regardless of high freq to low freq or on the other hand), adding 6 instructions delay (NOP) is required.*

6. *Offset voltage will effect ADC's result, please refer to figure 16 to detail.*

I. General Description

The EM785830AA is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. There are 16Kx13 bits ROM within it.

This integrated single chip has an on_chip watchdog timer (WDT, data RAM, programmable real time clock/counter, internal interrupt, power down mode, 4-channel 10-bit A/D converter, two channel PWM output, SPI and tri-state I/O.

II. Feature

CPU

・Operating voltage : 2.2V~5.5V at main CLK less then 3.58MHz.

Main CLK(Hz)	Under 3.58M	7.16M	10.74M	14.3M
Operating Voltage(min)	2.2	2.5	3	3.6

- 16k x 13 on chip Program Memory
- 0.5k x 8 on chip data RAM
- Up to 21 bi-directional tri-state I/O ports(4 shared with AD input; 1 shared with external interrupt input)
- 12 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- Two 8-bit counters : COUNTER1 and COUNTER2
- On-chip watchdog timer (WDT)
- 99.9% single instruction cycle commands
- Four modes (Main clock can be programmed from 447.829k to 14.3MHz generated by internal PLL)

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- 7 level Normal mode frequency : 447.8K , 895.7K , 1.79M , 3.58M , 7.16M , 10.75M and 14.3MHz.
- Input port interrupt function
- Dual clocks operation (Internal PLL main clock , External 32.768KHz)

SPI

- Serial Peripheral Interface (SPI) : a kind of serial I/O interface
- Interrupt flag available for the read buffer full or transmitter buffer empty.
- Programmable baud rates of communication
- Three-wire synchronous communication. (shared with IO)

PWM

- Dual PWM (Pulse Width Modulation) with 10-bit resolution
- Programmable period (or baud rate)
- Programmable duty cycle

ADC

・Operating : 2.5V 5.5V

・4 channel 10-bit successive approximation A/D converter

・Internal (VDD) or external reference

POR

・Power-on voltage detector reset

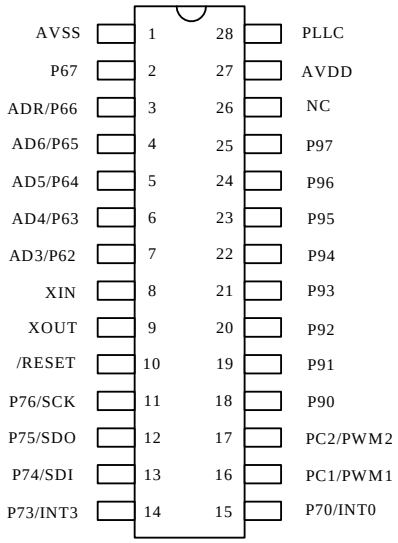
PACKAGE

EM78P5830AM, EM78P5830AAM, EM785830AAM → 28 pin SOP
EM78P5830AP, EM78P5830AAP, EM785830AAP → 28 pin PDIP

III. Application

General products

IV. Pin Configuration



EM785830AAP, EM785830AAM
EM78P5830AP, EM78P5830AM
EM78P5830AAP, EM78P5830AAM

Fig.1 Pin assignment

V. Functional Block Diagram

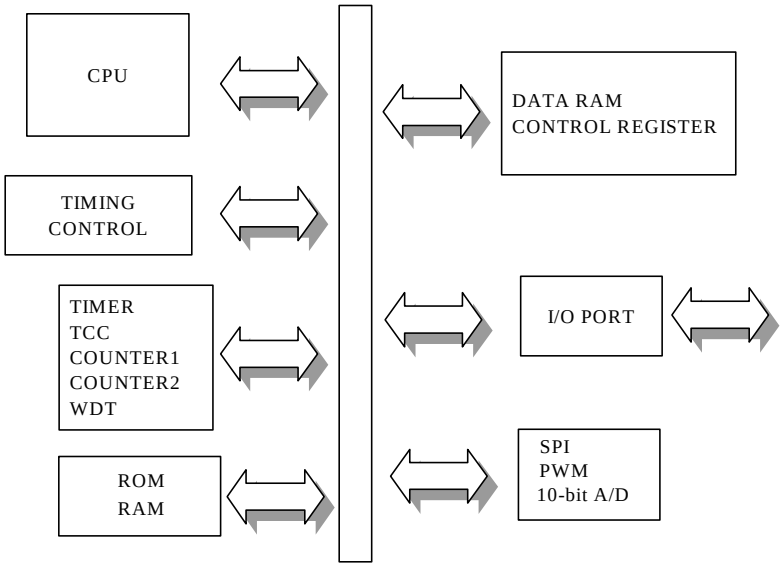


Fig.2a Block diagram

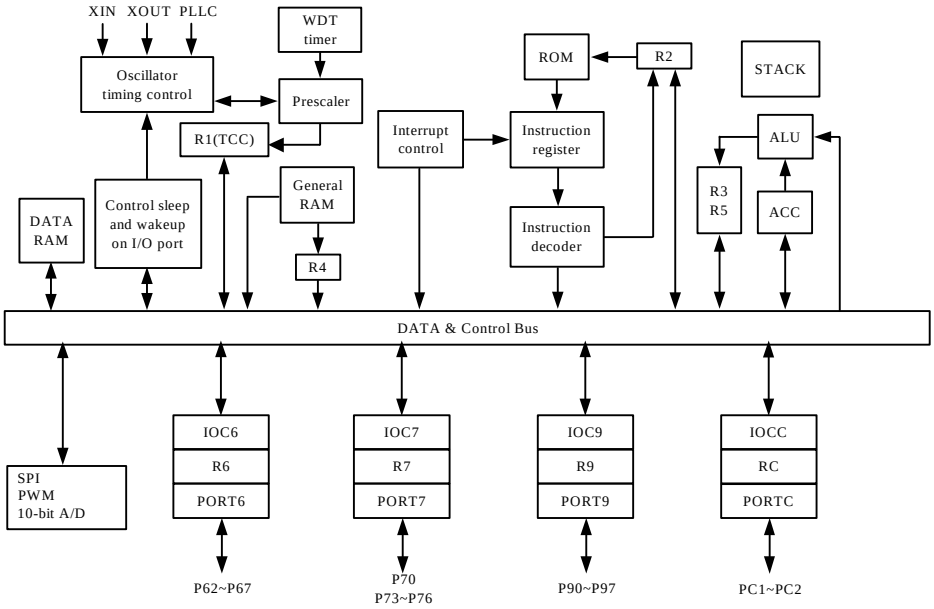


Fig.2b Block diagram

VI. Pin Descriptions

PIN	I/O	DESCRIPTION
POWER		
AVDD	POWER	Power
AVSS	POWER	Ground
CLOCK		
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.047u to 0.1u to the ground.
10-bit 4 channel A/D		
VREF	I (P66)	ADC reference input. Shared with PORT66
AD3	I (P62)	ADC input channel 3. Shared with PORT62
AD4	I (P63)	ADC input channel 4. Shared with PORT63
AD5	I(P64)	ADC input channel 5. Shared with PORT64
AD6	I(P65)	ADC input channel 6. Shared with PORT65
SPI		
SCK	IO (PORT76)	Master: output pin, Slave: input pin. This pin shared with PORT76.
SDO	O (PORT75)	Output pin for serial data transferring. This pin shared with PORT75.
SDI	I (PORT74)	Input pin for receiving data. This pin shared with PORT74.
PWM		
PWM1	O	Pulse width modulation output channel 1 This pin shared with PORTC1
PWM2	O	Pulse width modulation output channel 2 This pin shared with PORTC2
IO		
P62 ~P67	I/O	PORT6 can be INPUT or OUTPUT port each bit.
P70 ; P73~P76	I/O	PORT7 can be INPUT or OUTPUT port each bit.
P90 ~ P97	I/O	PORT9 can be INPUT or OUTPUT port each bit.
PC1 ~ PC2	I/O	PORTC can be INPUT or OUTPUT port each bit.
INT0	PORT70	Interrupt sources. Once PORT70 has a falling edge or rising edge signal (controlled by CONT register), it will generate a interruption.
INT3	PORT73	Interrupt sources which has the same interrupt flag. Any pin from PORT73 has a falling edge signal, it will generate a interruption.
/RESET	I	Low reset

VII. Functional Descriptions

VII.1 Operational Registers

Register configuration

	R PAGE registers			
Addr	R PAGE0	R PAGE1	R PAGE2	R PAGE3
00	Indirect addressing			
01	TCC			
02	PC			
03	Page, Status			
04	RAM bank, RSR			
05	Port5 I/O data, Program ROM page		SPI control	PWM control
06	Port6 I/O data		SPI data buffer	Duty of PWM1
07	Port7 I/O data	Data RAM bank		PWM1 control Duty of PWM1
08		Data RAM address		Period of PWM1
09	Port9 I/O data	Data RAM data buffer		Duty of PWM2
0A	PLL, Main clock, WDTE			PWM2 control Duty of PWM2
0B		ADC output data buffer		Period of PWM2
0C	PortC I/O data	Counter1 data		
0D		Counter2 data		
0E	Interrupt flag			
0F	Interrupt flag			
10	16 bytes Common registers			
:				
1F				
20	Bank0~Bank3 Common registers (32x8 for each bank)			
:				
3F				

	IOC PAGE registers	
Addr	IOC PAGE0	IOC PAGE1
00		
01		
02		
03		
04		
05	Port5 I/O control,	
06	Port6 I/O control	Port6 switches
07	Port7 I/O control	Port7 pull high
08		
09	Port9 I/O control	
0A		
0B		ADC control
0C	PortC I/O control	
0D		Clock source(CN1,CN2) Prescaler(CN1,CN2)

0E		
0F	Interrupt mask	
10		
:		
1F		
20		
:		
3F		

VII.2 Operational Register Detail Description

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov    A, @0x20        ;store a address at R4 for indirect addressing
Mov    0x04, A
Mov    A, @0xAA        ;write data 0xAA to R20 at bank0 through R0
Mov    0x00, A
```

R1 (TCC)

TCC data buffer. Increased by 16.384KHz or by the instruction cycle clock (controlled by CONT register). Written and read by the program as any other register.

R2 (Program Counter)

The structure is depicted in Fig.3.

Generates 16k × 13 on-chip ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A11) will be loaded with the contents of bit PS0~PS1 in the status register (R5 PAGE0) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.

If an interrupt is triggered, PROGRAM ROM will jump to address 0x08 at page0. The CPU will store ACC, R3 status and R5 PAGE automatically, and they will be restored after instruction RETI.

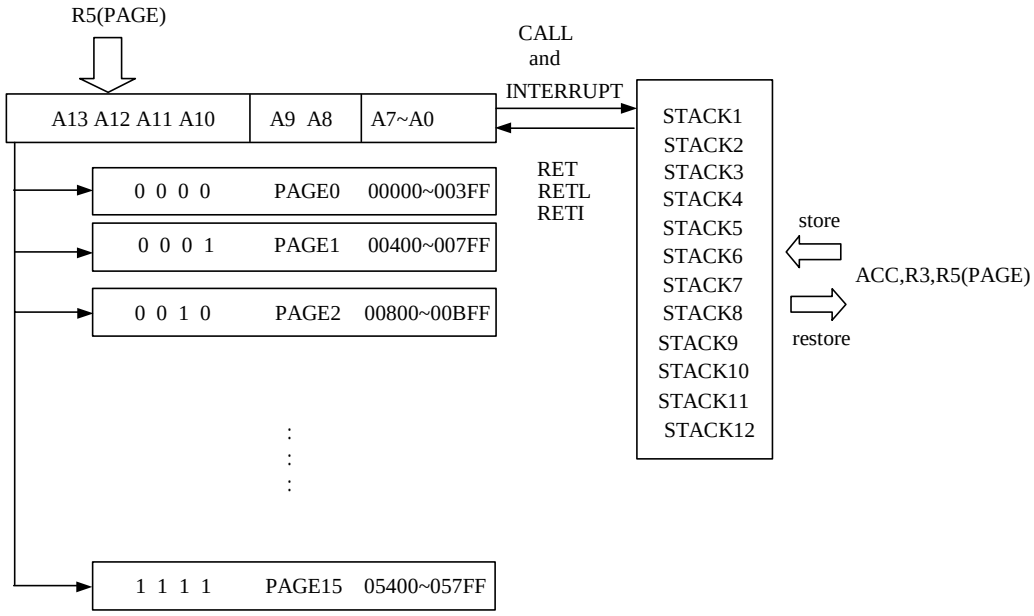


Fig.3 Program counter organization

R3 (Status, Page selection)

(Status flag, Page selection bits)

7	6	5	4	3	2	1	0
RPAGE1	RPAGE0	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0(C) : Carry flag

Bit 1(DC) : Auxiliary carry flag

Bit 2(Z) : Zero flag

Bit 3(P) : Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4(T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	X	x : don't care

Bit 5(IOCPAGE) : change IOC5 ~ IOCE to another page

Please refer to Fig.4 control register configuration for details.

0/1 ➔ IOC page0 / IOC page1

Bit 6(RPAGE0 ~ RPAGE1) : change R5 ~ RE to another page

Please refer to VII.1 Operational registers for detail register configuration.

(RPAGE1,RPAGE0)	R page # selected
(0,0)	R page 0
(0,1)	R page 1
(1,0)	R page 2
(1,1)	R page 3

R4 (RAM selection for common registers R20 ~ R3F))

(RAM selection register)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F).

Please refer to VII.1 Operational registers for details.

R5 (PORT5 I/O data, Program page selection, SPI control , PWM control)

PAGE0 (PORT5 I/O data register, Program page register)

7	6	5	4	3	2	1	0
-	-	-	-	PS3	PS2	PS1	PS0
				R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (PS0 ~ PS3): Program page selection bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

User can use PAGE instruction to change page to maintain program page by user.

Bit 4: (undefined) not allowed to use. This bit must clear to 0 or some unpredicted wrong will occur.

Bit 5 ~ Bit 7: (undefined) not allowed to use. These bits are not sure be 0 or 1.

PAGE2 (SPI control)

7	6	5	4	3	2	1	0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (SBR0 ~ SBR2) : SPI baud rate selection bits

SBR2	SBR1	SBR0	Mode	Baud rate
0	0	0	Master	Fsco
0	0	1	Master	Fsco/2
0	1	0	Master	Fsco/4
0	1	1	Master	Fsco/8
1	0	0	Master	Fsco/16
1	0	1	Master	Fsco/32
1	1	0	Slave	
1	1	1	Master	16.384k

<Note> Fsco = CPU instruction clock

For example :

If PLL is enabled and main clock is selected to 3.5826MHz, the instruction clock is 3.5826MHz/2

➔ Fsco=3.5862MHz/2

If PLL is enabled and main clock is selected to 3.5826MHz, the instruction clock is 0.895MHz/2

➔ Fsco=0.895MHz/2
If PLL is disabled, the instruction clock is 32.768kHz/2 ➔ Fsco=32.768kHz/2.

Bit 3 (SCES) : SPI clock edge selection bit
1➔Data shifts out on falling edge, and shifts in on rising edge. Data is hold during the high level.
0➔Data shifts out on rising edge, and shifts in on falling edge. Data is hold during the low level.

Bit 4 (SE) : SPI shift enable bit
1 ➔ Start to shift, and keep on 1 while the current byte is still being transmitted.
0 ➔ Reset as soon as the shifting is complete, and the next byte is ready to shift.
<Note> This bit has to be reset in software.

Bit 5 (SRO) : SPI read overflow bit
1 ➔ A new data is received while the previous data is still being hold in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users had better to read SPIB register even if the transmission is implemented only.
0 ➔ No overflow, <Note> This can only occur in slave mode.

Bit 6 (SPIE) : SPI enable bit
1 ➔ Enable SPI mode
0 ➔ Disable SPI mode

Bit 7 (RBF) : SPI read buffer full flag
1 ➔ Receive is finished, SPIB is full.
0 ➔ Receive is not finish yet, SPIB is empty.

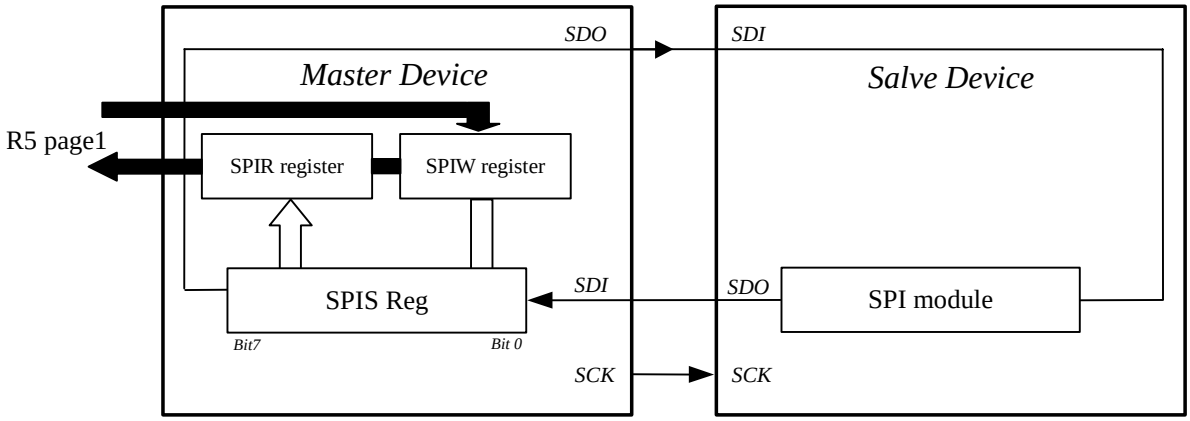


Fig.4 Single SPI Master / Salve Communication

Fig. 4 shows how SPI to communicate with other device by SPI module. If SPI is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted on a basis of both the clock rate and the selected edge.

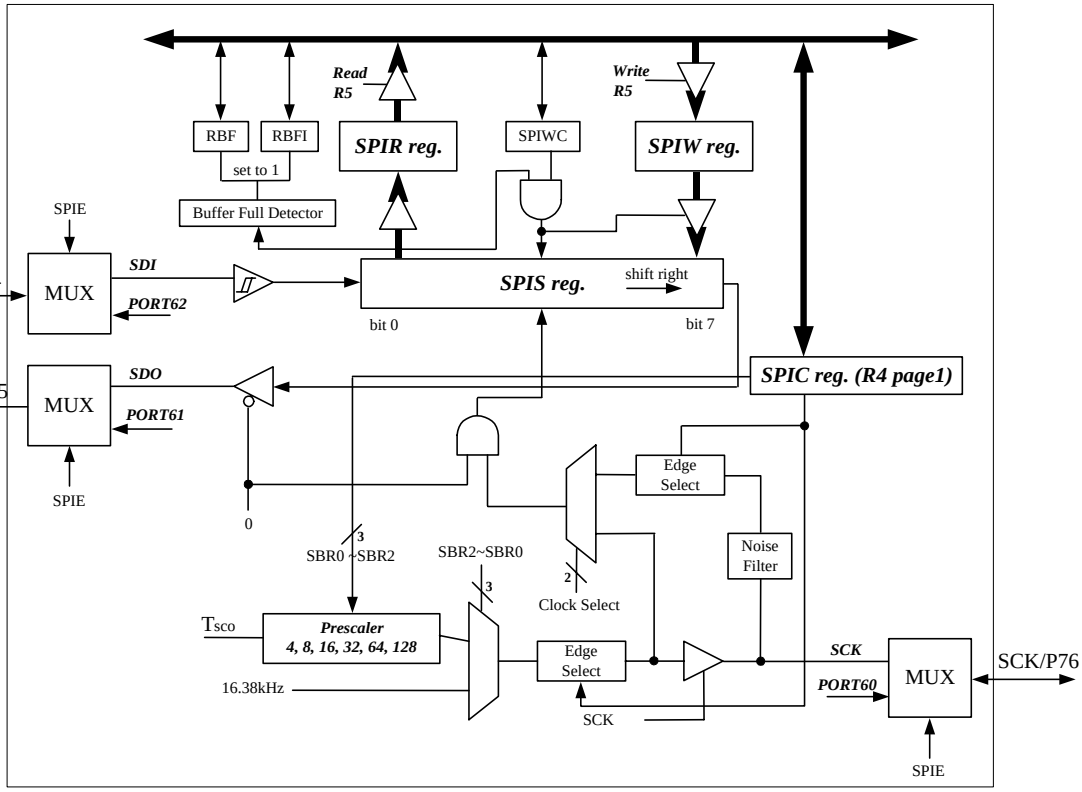


Fig.5 SPI structure

SPIC reg. : SPI control register
SDO: Serial data out
SDI: Serial data in
SCK: Serial clock
RBF : Set by buffer full detector, and reset in software.
RBFI : Interrupt flag. Set by buffer full detector, and reset in software.
Buffer Full Detector : Sets to 1, while an 8-bit shifting is complete.
SE : Loads the data in SPIW register, and begin to shift
SPIE : SPI control register
SPIS reg. : Shifting byte out and in.

The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data being written to, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shifting of the 8-bit data is complete. The RBF (Read Buffer Full) flag and the RBFI(Read Buffer Full Interrupt) flag are set.

SPIR reg. : Read buffer.

The buffer will be updated as the 8-bit shifting is complete. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register read.

SPIW reg. : Write buffer.

The buffer will deny any write until the 8-bit shifting is complete. The SE bit will be kept in 1 if the communication is still under going. This flag must be cleared as the shifting is finished. Users can determine if the next write attempt is available.

SBR2 ~ SBR0: Programming the clock frequency/rates and sources.
Clock select : Selecting either the internal instruction clock or the external 16.338KHz clock as the shifting clock.
Edge Select : Selecting the appropriate clock edges by programming the SCES bit

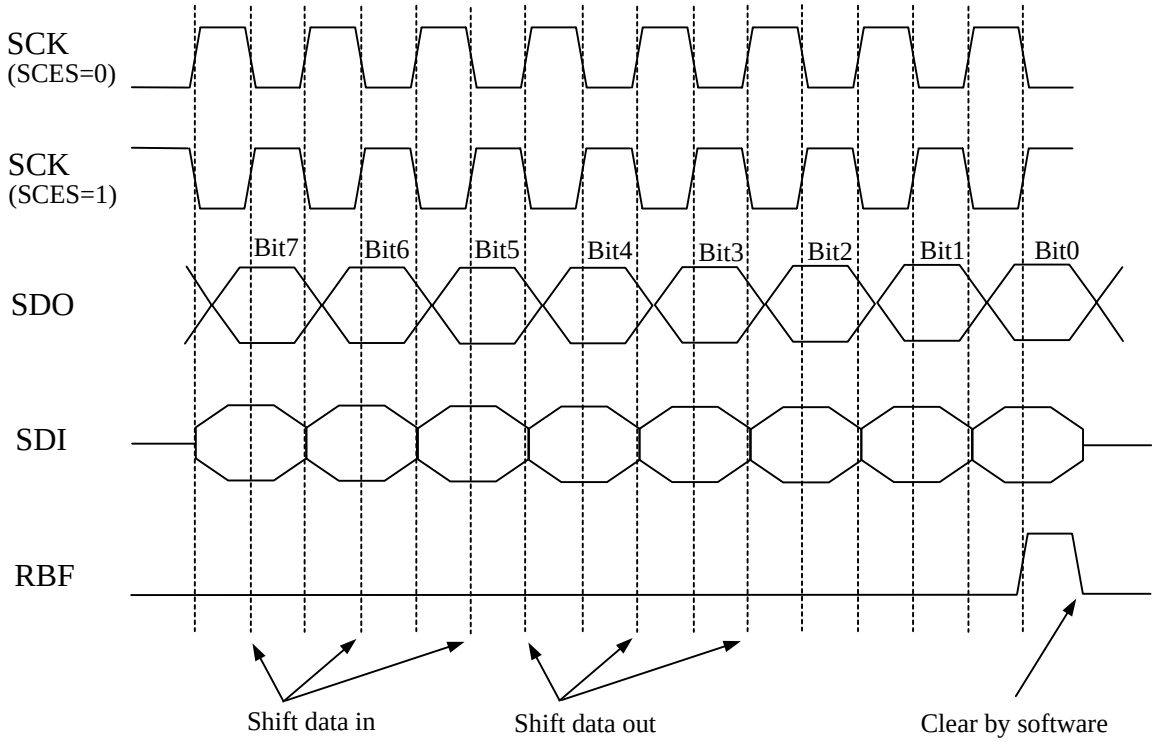


Fig.6 SPI timing

PAGE3 (PWMCON)

7	6	5	4	3	2	1	0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 1 (T1P0 ~ T1P1): TMR1 clock prescale option bits.

T1P1	T1P0	Prescale
0	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 2 ~ Bit 3 (T2P0 ~ T2P1): TMR2 clock prescale option bits.

T2P1	T2P0	Prescale
0	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 4 (T1EN): TMR1 enable bit
0 ➔ TMR1 is off (default value).
1 ➔ TMR1 is on.
Bit 5 (T2EN): TMR2 enable bit
0 ➔ TMR2 is off (default value).
1 ➔ TMR2 is on.

Bit 6 (PWM1E): PWM1 enable bit
0 ➔ PWM1 is off (default value), and its related pin carries out the PC1 function;
1 ➔ PWM1 is on, and its related pin will be set to output automatically.
Bit 7 (PWM2E): PWM2 enable bit
0 ➔ PWM2 is off (default value), and its related pin carries out the PC2 function.
1 ➔ PWM2 is on, and its related pin will be set to output automatically.

R6 (PORT6 I/O data, SPI data buffer)

PAGE0 (PORT6 I/O data register)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	X	X
R/W	R/W	R/W	R/W	R/W	R/W	-	-

Bit0 ~Bit1: Unused register. These two bits are not allowed to use.
Bit2 ~ Bit7 (P62 ~ P67) : 6-bit PORT6(2~7) I/O data register
User can use IOC register to define input or output each bit.

PAGE1 : (undefined) not allowed to use

PAGE2 (SPI data buffer)

7	6	5	4	3	2	1	0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer
If you write data to this register, the data will write to SPIW register. If you read this data, it will read the data from SPIR register. Please refer to figure7

PAGE3 (DT1L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle of PWM1)

7	6	5	4	3	2	1	0
PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

A specified value keeps the output of PWM1 to stay at high until the value matches with TMR1.

R7 (PORT7 I/O data, Data RAM bank)

PAGE0 (PORT7 I/O data register)

7	6	5	4	3	2	1	0
X	P76	P75	P74	P73	X	X	P70
-	R/W	R/W	R/W	R/W	-	-	R/W

Bit 0 ; Bit3 ~ Bit 7 (P73 ~ P76) : 5-bit PORT7 I/O data register
User can use IOC register to define input or output each bit.
Bit1~2, Bit 7: Unused register. These three bits are not allowed to use.

PAGE1 (Data RAM bank selection bits)

7	6	5	4	3	2	1	0
-	-	AD9	AD8		ADRES	0	RAM_B0
		R	R	-	R/W-0	R/W-0	R/W-0

Bit 0(RAM_B0) : Data RAM bank selection bits
Each bank has address 0 ~ address 255 which is total 256 (0.25k) bytes RAM size.
Data RAM bank selection : (Total RAM = 0.5K)

RAM_B0	RAM bank
0	Bank0
1	Bank1

Bit 1 : (undefined) not allowed to use. This bit must clear to 0.

Bit 2(ADRES) : Resolution selection for ADC

0 ➔ ADC is 8-bit resolution

When 8-bit resolution is selected, the most significant(MSB) 8-bit data output of the internal 10-bit ADC will be mapping to RB PAGE1 so R7 PAGE1 bit 4 ~5 will be of no use.

1 ➔ ADC is 10-bit resolution

When 10-bit resolution is selected, 10-bit data output of the internal 10-bit ADC will be exactly mapping to RB PAGE1 and R7 PAGE1 bit 4 ~5.

Bit 3 : (undefined) not allowed to use

Bit 4 ~ Bit 5(AD8 ~ AD9) : The most significant 2 bit of 10-bit ADC conversion output data

Combine these two bits and RB PAGE1 as complete 10-bit ADC conversion output data.

Bit 6 ~ Bit 7: (undefined) not allowed to use.

PAGE2 : (undefined) not allowed to use

PAGE3 (DT1H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle of PWM1)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PWM1[9]	PWM1[8]
						R/W-0	R/W-0

Bit 0 ~ Bit 1 (PWM1[8] ~ PWM1[9]): The Most Significant Byte of PWM1 Duty Cycle

A specified value keeps the PWM1 output to stay at high until the value matches with TMR1.

Bit 2 Bit 7 : unused

R8 (Data RAM address, PWM1 period)

PAGE0: (undefined) not allowed to use

PAGE1 (Data RAM address register)

7	6	5	4	3	2	1	0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (RAM_A0 ~ RAM_A7) : data RAM address

The data RAM bank's selection is from R7 PAGE1 bit0 (RAM_B0).

PAGE2: (undefined) not allowed to use)

PAGE3(PRD1): Period of PWM1

7	6	5	4	3	2	1	0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

The content of this register is a period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

R9 (PORT9 I/O data, Data RAM data buffer)

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (Data RAM data register)

7	6	5	4	3	2	1	0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (RAM_D0 ~ RAM_D7) : Data RAM's data register.

The address for data RAM is accessed from R8 PAGE1. The data RAM bank is selected by R7 PAGE1 Bit0 (RAM_B0).

PAGE2 : (undefined) not allowed to use

PAGE3 (DT2L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle of PWM2)

7	6	5	4	3	2	1	0
PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

A specified value keeps the output of PWM2 to stay at high until the value matches with TMR2.

RA (PLL, Main clock selection, Watchdog timer)

PAGE0 (PLL enable bit, Main clock selection bits, Watchdog timer enable bit)

7	6	5	4	3	2	1	0
0	PLLEN	CLK2	CLK1	CLK0	X	X	WDTEN
R/W-0	R/W-0	R/W	R/W	R/W	-	-	R/W-0

Bit 0(WDTEN) : Watch dog control bit

User can use WDTC instruction to clear watch dog counter. The counter 's clock source is 32768/2 Hz. If the prescaler assigns to TCC. Watch dog will time out by (1/32768)*2 * 256 = 15.616mS. If the prescaler assigns to WDT, the time of time out will be more times depending on the ratio of prescaler.

0/1 ➔ disable/enable

Bit 1~Bit 2 : Unused, these 2 bits are not allowed to use.

Bit 3 ~ Bit 5 (CLK0 ~ CLK2) : MAIN clock selection bits

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK2	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791MHz	1.791MHz (Normal mode)
1	0	1	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	1	0	0	32.768kHz	7.165MHz	7.165MHz (Normal mode)
1	1	0	1	32.768kHz	10.747MHz	10.747MHz (Normal mode)
1	1	1	0	32.768kHz	14.331MHz	14.331MHz (Normal mode)
1	1	1	1	***Can't allowed to use***		
0	don't care	don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)

Bit 6(PLLEN) : PLL's power control bit which is CPU mode control register

0/1 ➔ disable PLL/enable PLL

If enable PLL, CPU will operate at normal mode (high frequency). Otherwise, it will run at green mode (low frequency, 32768 Hz).

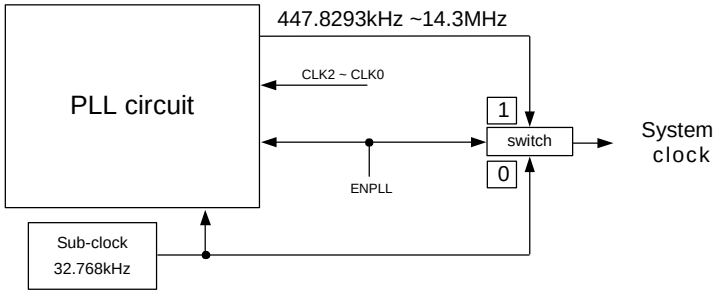


Fig.7 The relation between 32.768kHz and PLL

Bit 7: Unused register. Always keep this bit to 0 or some un-expect error will happen!

The status after wake-up and the wake-up sources list as the table below.

Wakeup signal	SLEEP mode
	RA(7,6)=(0,0) + SLEP
TCC time out IOCF bit0=1	No function
COUNTER1 time out IOCF bit1=1	No function
COUNTER2 time out IOCF bit2=2	No function
WDT time out	Reset and jump to address 0
PORT7 (0,3)	Reset and Jump to address 0

<Note> PORT70 's wakeup function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).

PORT73 's wakeup function is controlled by IOCF bit 5. It is falling edge trigger.

PAGE1,2 : (undefined) not allowed to use

PAGE3 (DT2H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle of PWM2)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PWM2[9]	PWM2[8]
						R/W-0	R/W-0

Bit 0 ~ Bit 1 (PWM2[8] ~ PWM2[9]): The Most Significant Byte of PWM1 Duty Cycle
A specified value keeps the PWM1 output to stay at high until the value matches with TMR1.
Bit 2 ~ Bit 7 : unused

RB (ADC input data buffer)

PAGE0 : (undefined) not allowed to use

PAGE1 (ADC output data register)

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (AD0 ~ AD7) : The last significant 8 bit of 10-bit or whole of 8 bit resolution ADC conversion output data. Combine there 8 bits and R7 PAGE1 bit4~5 as complete 10-bit ADC conversion output data in 10 bit resolution mode.

PAGE2 (undefined) not allowed to use. **This page is not sure to be 0 or 1**

PAGE3 (PRD2: Period of PWM2)

7	6	5	4	3	2	1	0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

The content of this register is a period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

RC (PORTC I/O data, Counter1 data)

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
X	X	X	X	X	PC2	PC1	X
-	-	-	-	-	R/W	R/W	-

Bit 1 ~ Bit 2 (PC1 ~ PC2): PORTC1,PORTC2 I/O data register

User can use IOC register to define input or output each bit.

Bit 0; Bit 3~Bit 7: (undefined) not allowed to use. **These bits are not sure to 0 or 1**

PAGE1 (Counter1 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17) : Counter1's buffer that user can read and write.

Counter1 is a 8-bit up-counter with 8-bit prescaler that user can use RC PAGE1 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

Example for writing :

```
MOV   0x0C, A   ; write the data at accumulator to counter1 (preset)
```

Example for reading :

```
MOV   A, 0x0C    ; read the data at counter1 to accumulator
```

PAGE2,3 (undefined) not allowed to use. **This page is not sure to 0 or 1**

RD (Counter2 data)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
X	***0***	***0***	***1***	X	***0***	***0***	***0***
-	R/W-0	R/W-0	R/W-0	-	R/W	R/W	R/W

Bit 0 ~Bit 2 : These three bits must clear to 0 or MCU power consumption will increase.

Bit 3 , Bit 7 : (undefined) not allowed to use

Bit4 ~ Bit6: These 3 bits are unused, please clear bit5 and bit6 to 0 and set bit4 to 1.

PAGE1 (Counter2 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN20 ~ CN27) : Counter2's buffer that user can read and write.

Counter2 is a 8-bit up-counter with 8-bit prescaler that user can use RD PAGE1 to preset and read the counter.(write ➔ preset) After a interruption, it will reload the preset value.

Example for writing :

```
MOV   0x0D, A   ; write the data at accumulator to counter2 (preset)
```

Example for reading :

```
MOV   A, 0x0D   ; read the data at counter2 to accumulator
```

PAGE2,3 (undefined) not allowed to use. **This page is not sure to 0 or 1**

RE (Interrupt flag)

PAGE0 (Interrupt flag)

7	6	5	4	3	2	1	0
PWM2	RBF	ADI	PWM1	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit0 ~ Bit3 : These three bits must clear to 0 or unable to expect error will occur .

Bit 4(PWM1) : PWM1 one period reach interrupt flag.

Bit 5 (ADI) : ADC interrupt flag after a sampling

Bit 6 (RBF) : SPI data transfer complete interrupt

If SPI's RBF signal has a rising edge signal (RBF set to "1" when transfer data completely), CPU will set this bit.

Bit 7(PWM2) : PWM2 one period reach interrupt flag.

PAGE2,3 (undefined) not allowed to use. **This page is not sure to 0 or 1**

RF (Interrupt status)

(Interrupt status register)

7	6	5	4	3	2	1	0
INT3	-	-	-	INT0	CNT2	CNT1	TCIF
R/W-0				R/W-0	R/W-0	R/W-0	R/W-0

"1" means interrupt request, "0" means non-interrupt

Bit 0(TCIF) : TCC timer overflow interrupt flag

Set when TCC timer overflows.

Bit 1(CNT1) : counter1 timer overflow interrupt flag

Set when counter1 timer overflows.

Bit 2(CNT2) : counter2 timer overflow interrupt flag

Set when counter2 timer overflows.

Bit 3(INT0) : external INT0 pin interrupt flag

If PORT70 has a falling edge/rising edge (controlled by CONT register) trigger signal, CPU will set this bit.

Bit 4~6: Unused (These bits are not sure to 0 or 1. When programmer determine what interrupt occur in subroutine, be care to note these bits)

Bit 7(INT3) : external PORT73 pin interrupt flag

<Note> IOCF is the interrupt mask register. User can read and clear.

Trigger edge as the table

Signal	Trigger
TCC	Time out
COUNTER1	Time out
COUNTER2	Time out
INT0	Falling Rising edge
INT3	Falling edge

R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : all are general purpose registers.

VII.3 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
P70EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 ➔ TCC/WDT

Bit 4(RETBK) : Return value backup control for interrupt routine

0/1 ➔ disable/enable

When this bit is set to 1, the CPU will store ACC,R3 status and R5 PAGE automatically after an interrupt is triggered. And it will be restored after instruction RETI. When this bit is set to 0, the user need to store ACC, R3 and R5 PAGE in user program.

Bit 5(TS) : TCC signal source

0 ➔ internal instruction cycle clock

1 ➔ 16.384kHz

Bit 6 (INT) : INT enable flag

0 ➔ interrupt masked by DISI or hardware interrupt

1 ➔ interrupt enabled by ENI/RETI instructions

Bit 7(P70EG) : interrupt edge type of P70

0 ➔ P70 's interruption source is a rising edge signal.

1 ➔ P70 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

TCC and WDT :

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.

See the prescaler ratio in CONT register.

Fig.8 depicts the circuit diagram of TCC/WDT.

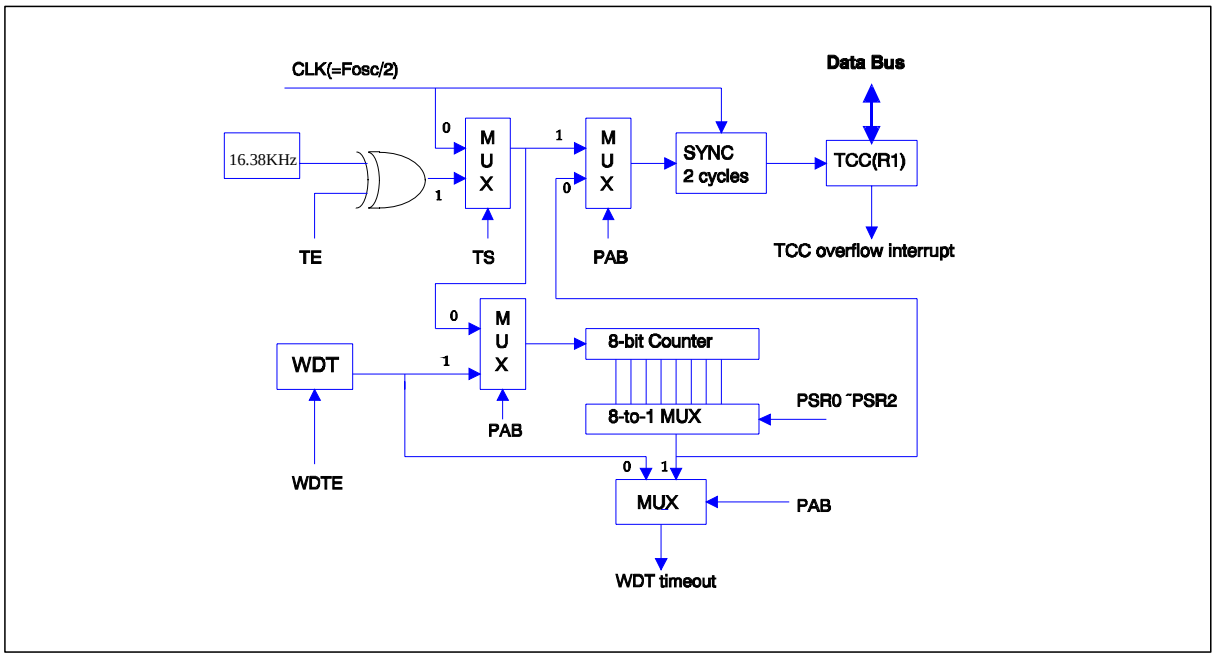


Fig.8 Block diagram of TCC WDT

IOC5 (Unused)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	X	X	X	X	X
R/W	R/W	R/W	-	-	-	-	-

Bit0~4 : *(undefined) not allowed to use*

Bit5~Bit7(Unused) : These three bits must clear to 0 or MCU power consumption will increase.
The default value in these 3 bits are "1". Please clear them to "0" when init MCU.

PAGE1 (undefined) not allowed to use.**(This page is not sure to 0 or 1)**

IOC6 (PORT6 I/O control, P6* pins switch control)

PAGE0 (PORT6 I/O control register)

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	***0***	***0***
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit0~Bit1 (Unused) : These two bits must clear to 0 or MCU power consumption will increase.
The default value in these 2 bits are "1". Please clear them to "0" when init MCU.

Bit 2 ~ Bit 7 (IOC62 ~ IOC67) : PORT6(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (P6* pins switch control register)

7	6	5	4	3	2	1	0
-	P66S	P65S	P64S	P63S	P62S	0	0
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 1 : These 2 bits are undefined bits. Please clear them to 0.

Bit 2(P62S) : Select normal I/O PORT62 pin or channel 3 input AD3 pin of ADC

0 ➔ P62 (I/O PORT62) pin is selected

1 ➔ AD3 (Channel 3 input of ADC) pin is selected

Bit 3(P63S) : Select normal I/O PORT63 pin or channel 4 input AD4 pin of ADC

0 ➔ P63 (I/O PORT63) pin is selected

1 ➔ AD4 (Channel 4 input of ADC) pin is selected

Bit 4(P64S) : Select normal I/O PORT64 pin or channel 5 input AD5 pin of ADC

0 ➔ P64 (I/O PORT64) pin is selected

1 ➔ AD5 (Channel 5 input of ADC) pin is selected

Bit 5(P65S) : Select normal I/O PORT65 pin or channel 6 input AD6 pin of ADC

0 ➔ P65 (I/O PORT65) pin is selected

1 ➔ AD5 (Channel 6 input of ADC) pin is selected

Bit 6(P66S) : Select modulation transmitting output pin of AD or I/O PORT66 pin

0 ➔ P66 (I/O PORT66) pin is selected and ***ADC reference voltage come from internal VDD***

1 ➔ VREF (External reference voltage input of ADC) pin is selected, ***ADC reference voltage come from pin "ADR".***

IOC7 (PORT7 I/O control, PORT7 pull high control)

PAGE0 (PORT7 I/O control register)

7	6	5	4	3	2	1	0
0	IOC76	IOC75	IOC74	IOC73	0	0	IOC70
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit1~Bit2; Bit7 (Unused) : These 3 bits must clear to 0 or MCU power consumption will increase.

The default value in these 3 bits are "1". Please clear them to "0" when init MCU.

Bit 0 ; Bit3~Bit6 (IOC70; IOC73~IOC76) : PORT7 I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (PORT7 pull high control register)

7	6	5	4	3	2	1	0
0	PH76	PH75	PH74	PH73	0	0	PH70
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit1~Bit2; Bit7 (Unused) : These3 bits must clear to 0 or MCU power consumption will increase.

Bit0 ; Bit3~Bit6 : PORT7 pull high control register

0 ➔ disable pull high function.

1 ➔ enable pull high function

IOC8 (Unused)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	***0***	***0***	***0***
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

***** This page must clear to 0 or MCU power consumption will increase.***

The default value in these 8 bits are "1". Please clear them to "0" when init MCU.

PAGE1 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	***0***	***0***	***0***
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

***** This page must clear to 0 or the power consumption of MCU will increase.***

IOC9 (PORT9 I/O control, PORT9 switches)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	***0***	***0***	***0***
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

*****These 8 bits must clear to 0 or Port9 input or output function will wronging***

IOCA (Unused)

PAGE0(undefined) not allowed to use

PAGE1(undefined) not allowed to use

7	6	5	4	3	2	1	0
X	***0***	X	X	***0***	X	0	0
-	R/W	-	-	R/W	-	R/W-0	R/W-0

Bit0~Bit1 : Undefined registers. Please clear these two bits to 0.

Bit3 , Bit6 (Unused) : These 2 bits must clear to 0 or MCU power consumption will increase.

Bit2, 4,5,6 are undefined register, they are not allowed to use.

IOCB (ADC control)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	***0***	***0***	***0***
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

***** This page must clear to 0 or MCU power consumption will increase.***

The default value in these 8 bits are "1". Please clear them to "0" when init MCU.

PAGE1 (ADC control bits)

7	6	5	4	3	2	1	0
IN2	IN1	IN0	ADCLK1	ADCLK0	ADPWR	X	ADST
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	-	R/W-0

Bit 0(ADST) : AD converter start to sample

By setting to "1", the AD will start to sample data. This bit will be cleared by hardware automatically after a sampling.

Bit 1 : (undefined) not allowed to use

Bit 2(ADPWR) : AD converter power control, 1/0 ➔ enable/disable

Bit 3 ~ Bit 4 (ADCLK0 ~ ADCLK1) : AD circuit 's sampling clock source.

For PLL clock = 895.658kHz ~ 14.3MHz (CLK2~CLK0 = 001 ~ 111)

ADCLK1	ADCLK0	Sampling rate	Operation voltage
0	0	74.6K	>=3.5V
0	1	37.4K	>=3.0V
1	0	18.7K	>=2.5V
1	1	9.3K	>=2.5V

For PLL clock = 447.829kHz (CLK2~CLK0 = 000)

ADCLK1	ADCLK0	Sampling rate	Operation voltage
0	0	37.4K	>=3.0V
0	1	18.7K	>=3.0V
1	0	9.3K	>=2.5V
1	1	4.7K	>=2.5V

This is a CMOS multi-channel 10-bit successive approximation A/D converter.

Features

74.6kHz maximum conversion speed at 5V.
Adjusted full scale input
External reference voltage input or internal(VDD) reference voltage
4 analog inputs multiplexed into one A/D converter
Power down mode for power saving
A/D conversion complete interrupt
Interrupt register, A/D control and status register, and A/D data register

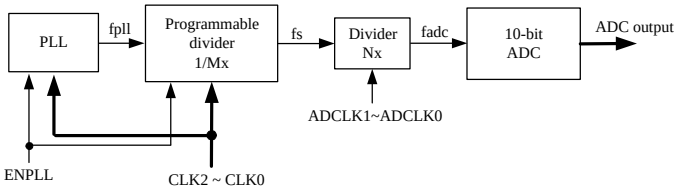


Fig.9 ADC voltage control logic

fpll	Mx	fs	fadcon = fadc / 12			
			Nx = 1	Nx = 2	Nx = 4	Nx = 8
14.331MHz	16	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
10.747MHz	12	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
7.165MHz	8	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
3.582MHz	4	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
1.791MHz	2	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
895.658kHz	1	895.658kHz	74.638kHz	37.391kHz	18.659khz	9.329kHz
447.829kHz	1	447.829kHz	37.391kHz	18.659khz	9.329kHz	4.665kHz

Bit 5 ~ Bit 7(IN0~ IN2) : Input channel selection of AD converter

These two bits can choose one of three AD input.

IN2	IN1	IN0	Input	Pin
0	0	0	-	Not select
0	0	1	-	Not select
0	1	0	AD3	P62
0	1	1	AD4	P63
1	0	0	AD5	P64
1	0	1	AD6	P65
1	1	0	-	Not select
1	1	1	-	Not select

IOCC (PORTC I/O control, ADC control)

PAGE0 (Unused)

7	6	5	4	3	2	1	0
0	***0***	***0***	***0***	***0***	IOCC2	IOCC1	***0***
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 1 ~ Bit 2 (IOCC1 ~ IOCC2) : PORTC(1~2) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

***** Bit0 , Bit3 ~ Bit7 must clear to 0 or MCU power consumption will increase.***

The default value in these 6 un-define bits are "1". Please clear them to "0" when init MCU.

PAGE1 (PORT switch)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	MS
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W/0

Bit 0(MS) : P6* switch mode selection

0 ➔ (default unknown)

1 ➔ ADC input mode selection

(Always set this bit to "1" otherwise partial ADC function cannot be used)

Bit 1 ~ Bit 7: (undefined) not allowed to use

IOCD (Clock source, Prescaler of CN1 and CN2)

PAGE0 (Reserved)

PAGE1 (Clock source and prescaler for COUNTER1 and COUNTER2)

7	6	5	4	3	2	1	0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2) : COUNTER1 prescaler ratio

C1_PSC2	C1_PSC1	C1_PSC0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT1S) : COUNTER1 clock source

0/1 ➔ 16.384kHz/system clock

Bit 4 ~ Bit 6 (C2_PSC0 ~ C2_PSC2) : COUNTER2 prescaler ratio

C2_PSC2	C2_PSC1	C2_PSC0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7(CNT2S) : COUNTER2 clock source

0/1 ➔ 16.384kHz/system clock

IOCE (Interrupt mask,)

PAGE0 (Interrupt mask)

7	6	5	4	3	2	1	0
PWM2	RBF	ADI	PWM1	***0***	***0***	***0***	***0***
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 : Undefined register. Please clear these bits to 0.

Bit 4(PWM1) : PWM1 one period reach interrupt mask.

Bit 5 (ADI) : ADC conversion complete interrupt mask

0/1 ➔ disable/enable interrupt

There are four registers for A/D converter. Use one bit of interrupt control register (IOCE PAGE0 Bit5) for A/D conversion complete interrupt. The status and control register of A/D (IOCB PAGE1 and RE PAGE0 Bit5) responses the A/D conversion status or takes control on A/D. The A/D data register (RB PAGE1) stores A/D conversion result.

ADI bit in IOCE PAGE0 register is end of A/D conversion complete interrupt enable/disable. It enables/disables ADI flag in RE register when A/D conversion is complete. ADI flag indicates the end of an A/D conversion. The A/D converter sets the interrupt flag, ADI in RE PAGE0 register when a conversion is complete. The interrupt can be disabled by setting ADI bit in IOCE PAGE0 Bit5 to '0'.

The A/D converter has 4 analog input channels AD3~AD6 multiplexed into one sample and hold to A/D module. Reference voltage can be driven from VREF pin or internal power. The A/D converter itself is of an 8-bit successive approximation type and produces an 8-bit result in the RB PAGE1 data register. A conversion is initiated by setting a control bit ADST in IOCB PAGE1 Bit0. Prior to conversion, the appropriate channel must be selected by setting IN0~IN1 bits in RE register and allowed for enough time to sample data. Every conversion data of A/D need 12-clock cycle time. The minimum conversion time required is 13 us (73K sample rate). ADST Bit in IOCB PAGE1 Bit0 must be set to begin a conversion.

It will be automatically reset in hardware when conversion is complete. At the end of conversion, the START bit is cleared and the A/D interrupt is activated if ADI in IOCE PAGE0 Bit5 = 1. ADI will be set when conversion is complete. It can be reset in software.

If ADI = 0 in IOCE PAGE0 Bit5, when A/D start conversion by setting ADST(IOCB PAGE1 Bit0) = 1 then A/D will continue conversion without stop and hardware won't reset ADST bit. In this condition, ADI is deactived. After ADI in IOCE PAGE0 bit5 is set, ADI in RE PAGE0 bit5 will activate again.

To minimum operating current , all biasing circuits in the A/D module that consume DC current are power down when ADPWR bit in IOCB PAGE1 Bit2 register is a '0'. When ADPWR bit is a '1', A/D converter module is operating.

User has to set PORT62~PORT65 as AD converter input pin or bi-direction IO PORT

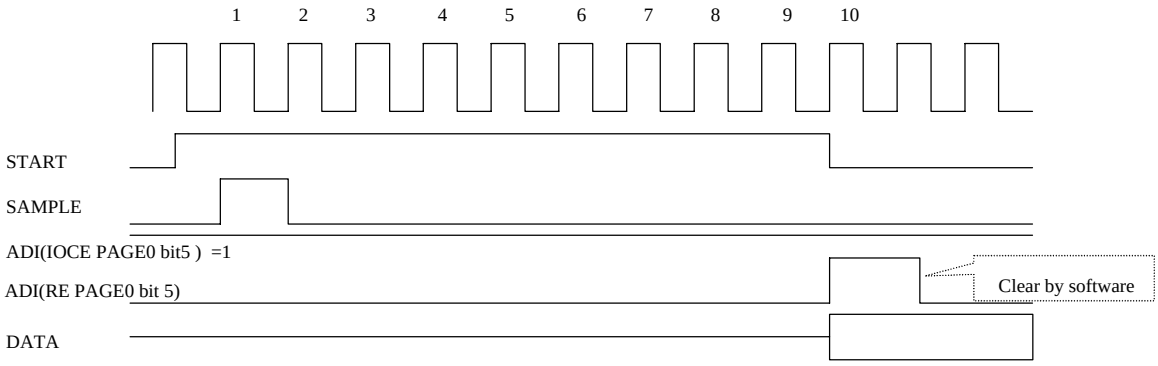


Fig.10 A/D converter timing

Bit 6 (RBF) : SPI's RBF interrupt mask

0/1 ➔ disable/enable interrupt

Bit 7(PWM2) : PWM2 one period reach interrupt mask.

IOCF (Interrupt mask)

(Interrupt mask register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT3	-	-	-	INT0	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 3 ; Bit 7 : interrupt enable bit

0 ➔ disable interrupt

1 ➔ enable interrupt

Bit 4~Bit6 : (remain these values to "0"othwise it will generate unpredicted interrupts)

The status after interrupt and the interrupt sources list as the table below.

Interrupt signal	GREEN mode	NORMAL mode
	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit0=1 And "ENI"	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER1 time out IOCF bit1=1 And "ENI"	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER2 time out IOCF bit2=2 And "ENI"	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
PORT70; 3 IOCF bit3 bit7 =1 And "ENI"	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
RBF IOCE bit6 = 1 And "ENI	Interrupt <ps> (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
ADI IOCE bit5 = 1 And "ENI	No function	Interrupt (jump to address 8 at page0)
PWM1 IOCE bit4 = 1 And "ENI	Interrupt <ps> (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
PWM2 IOCE bit7 = 1 And "ENI	Interrupt <ps> (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)

<Note> PORT70 's interrupt function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).

PORT73 's interrupt function is controlled by IOCF bit 7. They are falling edge trigger.

ADI interrupt source function is controlled by RE PAGE0 bit 5. It is rising edge trigger after ADC sample complete.

<ps> It only happens when master and 16.386kHz mode is selected.

VII.4 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.11.

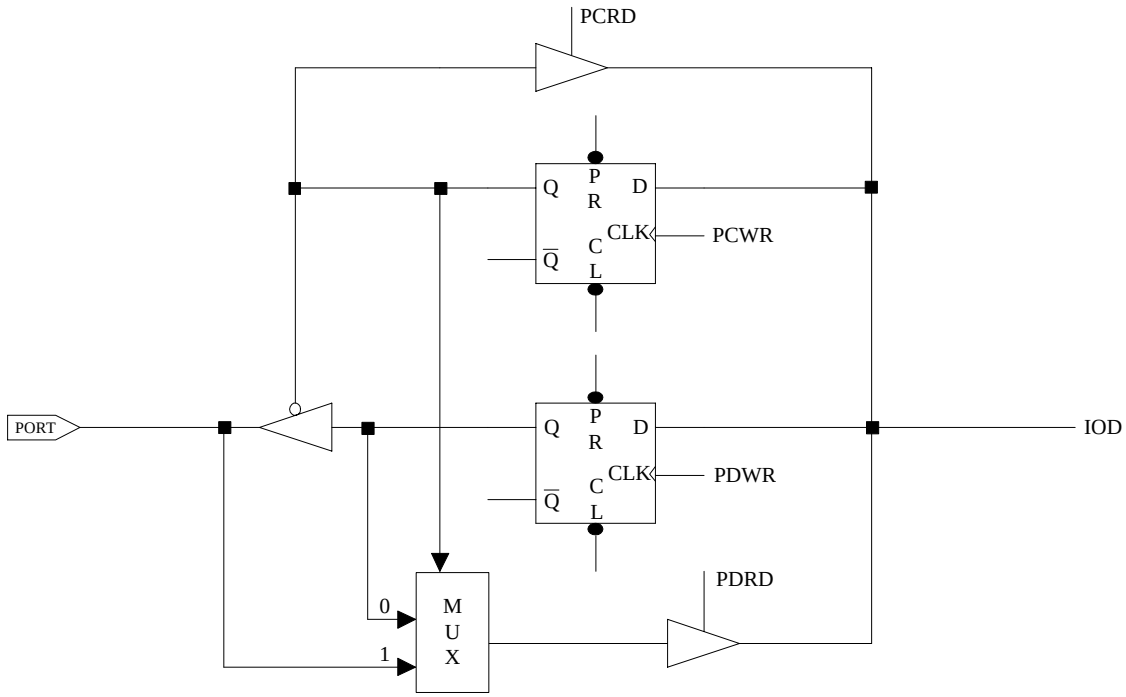


Fig.11_1 The circuit of I/O port and I/O control register

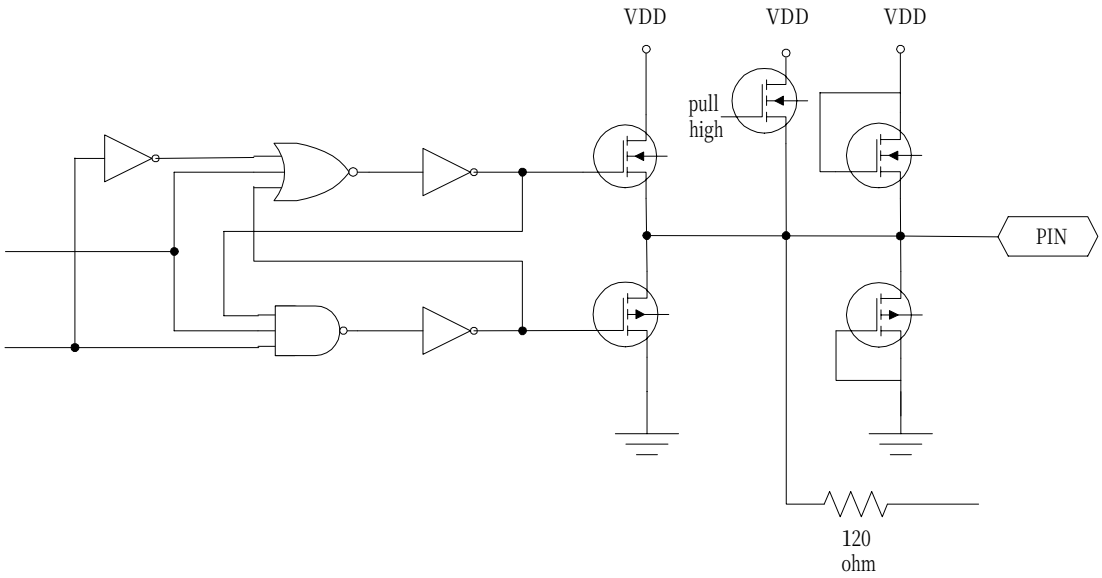


Fig.11_2 The input/output circuit of EM785830AA input/output ports

VII.5 RESET

The RESET can be caused by

(1) Power on reset

(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

(3) /RESET pin pull low

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit 7 ~ bit 0) default values are as follows.

Operation registers :

Address	R register PAGE0	R register PAGE1	R register PAGE2	R register PAGE3	IOC register PAGE0	IOC register PAGE1
0x4	00xxxxxx					
0x5	xxxx0000	xxxx0000	00000000	00000000	111x0000	
0x6	xxxxxxxx	xxxxxxxx	xxxxxxxx	00000000	11111111	00000000
0x7	xxxxxxxx	xxxx0000		xxxxxx00	11111111	00000000
0x8	xxxxxxxx	00000000		00000000	11111111	00000000
0x9	xxxxxxxx	xxxxxxxx		00000000	11111111	00000000
0xA	00011xx0	11111111	0x000000	xxxxxx00	xxxxxxxx	x0xx0xx
0xB	xxxxxxxx	xxxxxxxx	xxxxxxxx	00000000	11111111	000000x0
0xC	xxxxxxxx	00000000	xxxxxxxx		11111111	00000000
0xD	xxxxx000	00000000	xxxxxxxx		xxxxxxxx	00000000
0xE	00000000		xxxxxxxx		0000xxxx	xxxxxxxx
0xF	00000000				00000000	

VII.6 Wake-up

The controller provided sleep mode for power saving :

SLEEP mode, RA(7) = 0 + "SLEP" instruction

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has enable register), user has to turn it off by software.

Wake-up from SLEEP mode

(1) WDT time out

(2) External interrupt

(3) /RESET pull low

All these cases will reset controller , and run the program at address zero. The status just like the power on reset.

VII.7 Interrupt

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

VII.8 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1

0	0100	11rr	rrrr	04rr	COM R	/R → R	Z	1
0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z	1
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z	1
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None	1
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None	1
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None	1
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z	1
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1	1110	100k	kkkk	1E8k	PAGE k	K->R5(4:0)	None	1
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1

***** 1 Instruction cycle = 2 main CLK***

VII.9 Code Option

CODE Option Register

13	12	11	10	9	8	7	6	5	4	3	2	1	0
		0	***0***	***1***						MER			

Bit 3(MER) : Memory error recover function

0 ➔ disable memory error recover function

1 ➔ enable memory error recovery function

If user enable memory error recovery function, MCU will improve effect from environment noise**.**

Bit 9: This bit must set to 1.

Bit10 ~ Bit11 : These 2 bits must clear to 0.

VII.10 Dual sets of PWM (Pulse Width Modulation)

(1) Overview

In PWM mode, both PWM1 and PWM2 pins produce up to a 10-bit resolution PWM output (see. Fig.12 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Fig.13 depicts the relationships between a period and a duty cycle.

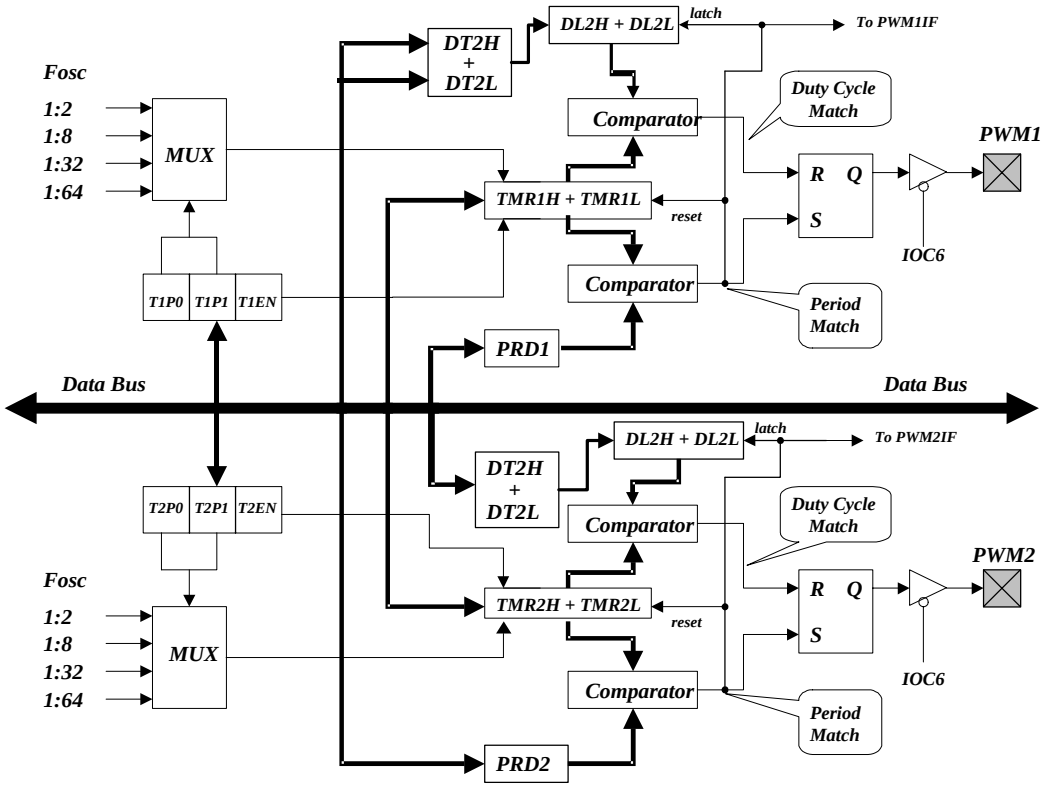


Fig.12 The Functional Block Diagram of the Dual PWMs

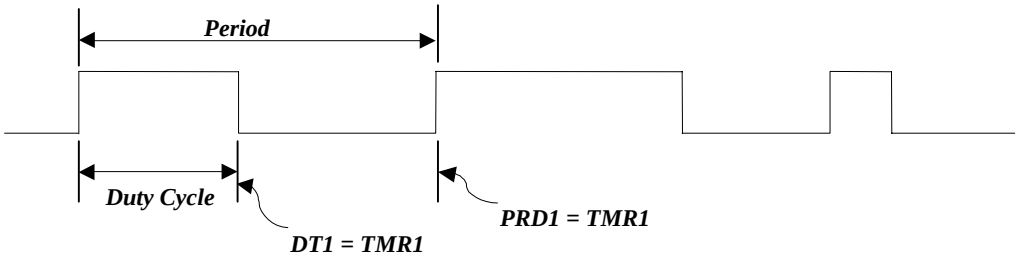


Fig.13 The Output Timing of the PWM

(2) Increment Timer Counter (TMRX: TMR1H/TWR1L or TMR2H/TWR2L)

TMRX are ten-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions. If employed, they can be turned down for power saving by setting T1EN bit [PWMCON<4>] or T2EN bit [PWMCON<5>] to 0.

(3) PWM Period (PRDX : PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:
• TMRX is cleared.
• The PWMX pin is set to 1.
• The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2.
< Note > The PWM output will not be set, if the duty cycle is 0;
• The PWMXIF pin is set to 1.
The following formula describes how to calculate the PWM period:
PERIOD = (PRDX + 1) * 4 * (1/Fosc) * (TMRX prescale value)
Where Fosc is system clock

(4) PWM Duty Cycle (DTX: DT1H/ DT1L and DT2H/ DT2L; DTL: DL1H/DL1L and DL2H/DL2L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DTL until the current value of DLX is equal to TMRX.
The following formula describes how to calculate the PWM duty cycle:
Duty Cycle = (DTX) * (1/Fosc) * (TMRX prescale value)

(5) PWM Programming Procedures/Steps

Load PRDX with the PWM period.
(1) Load DTX with the PWM Duty Cycle.
(2) Enable interrupt function by writing IOCF PAFE0, if required.
(3) Set PWMX pin to be output by writing a desired value to IOCC PAGE0.
(4) Load a desired value to R5 PAGE3 with TMRX prescaler value and enable both PWMX and TMRX.

(6) Timer

Timer1 (TMR1) and Timer2 (TMR2) (TMRX) are 10-bit clock counters with programmable prescalers, respectively. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions.
The figure in the next page shows TMRX block diagram. Each signal and block are described as follows:

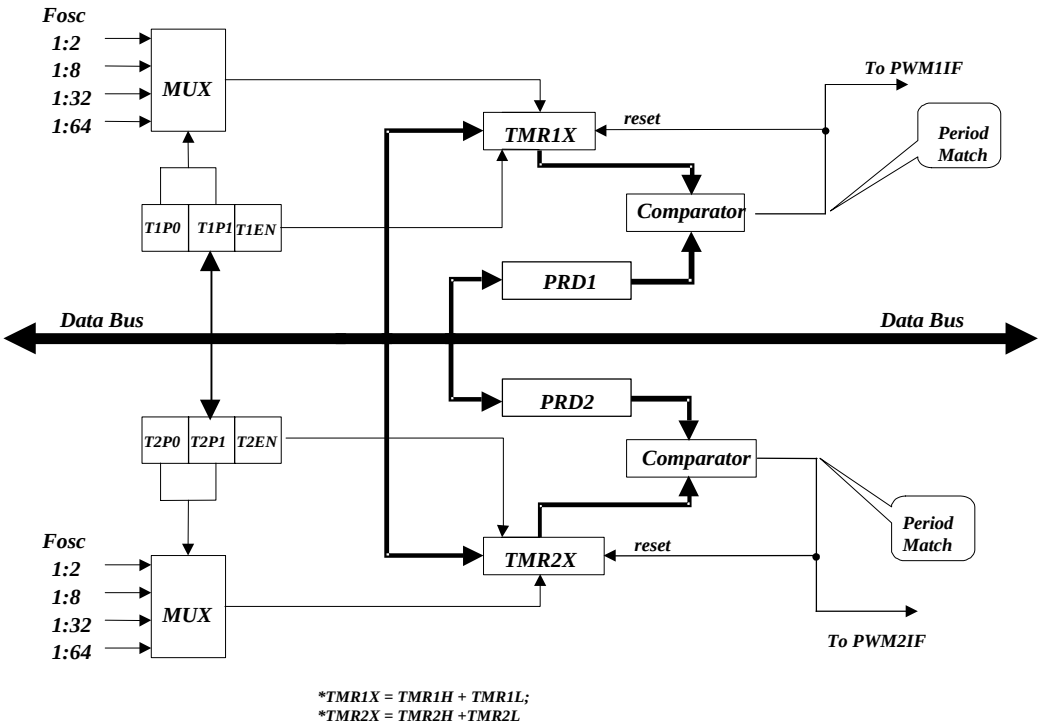


Fig.14 TMRX Block Diagram

- Fosc: Input clock.
- Prescaler (T1P0 and T1P1/T2P1 and T2P0): Options of 1:2, 1:8, 1:32, and 1:64 are defined by TMRX. It is cleared when any type of reset occurs.
- TMR1X and TMR2X (TMR1H/TWR1L and TMR2H/TMR2L):Timer X register; TMRX is increased until it matches with PRDX, and then is reset to 0. TMRX cannot be read.
- PRDX (PRD1 and PRD2): PWM period register.

When defining TMRX, refer to the related registers of its operation as shown in prescale register. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, bit 7 and bit 6 of the PWMCON register must be set to '0'.

Related Control Registers(R5 PAGE3) of TMR1 and TMR2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Timer programming procedures/steps

(1) Load PRDX with the TIMER period.
(2) Enable interrupt function by writing IOCF PAGE0, if required
(3) Load a desired value to PWMCON with the TMRX prescaler value and enable both TMRX and disable PWMX.

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	VDD	-0.3 To 6	V
INPUT VOLTAGE	Vin	-0.5 to VDD +0.5	V
OPERATING TEMPERATURE RANGE	Ta	0 to 70	℃

IX. DC Electrical Characteristic

(Ta = 25°C, AVDD=VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input leakage current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input leakage current for bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input high voltage	VIH		2.5			V
Input low voltage	VIL				0.8	V
Input high threshold voltage	VIHT	/RESET, TCC	2.0			V
Input low threshold voltage	VILT	/RESET, TCC			0.8	V
Clock input high voltage	VIHX	OSCI	3.5			V
Clock input low voltage	VILX	OSCI			1.5	V
Output high voltage for PORTC1~PORTC2	VOH1	IOH = -6mA	2.4			V
Output high voltage for PORT62~PORT67; PORT7	VOH2	IOH = -10mA	2.4			V
Output high voltage for PORT9	VOH3	IOH = -20mA	2.4			V
Output low voltage for PORTC1~PORTC2	VOL1	IOH = 6mA			0.4	V
Output low voltage for PORT62~PORT67; PORT7	VOL2	IOH = 10mA			0.4	V
Output low voltage for PORT9	VOL3	IOH = 20mA			0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS		-10	-15	μA
Power down current (SLEEP mode)	ISB1	All input and I/O pin at VDD, output pin floating, WDT disabled		4	8	μA
Low clock current (GREEN mode)	ISB2	CLK=32.768KHz, All analog circuits disabled, All input and I/O pin at VDD, output		35	50	μA
		pin floating, WDT disabled				
		pin floating, WDT disabled				
Operating supply current (Normal mode)	ICC1	/RESET=High, CLK=3.582MHz, All analog circuits disabled, output pin floating		1	2	mA

XI. AC Electrical Characteristic

CPU instruction timing (Ta = 25°C, AVDD=VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.582MHz		60 550		us ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note 1: N= selected prescaler ratio.

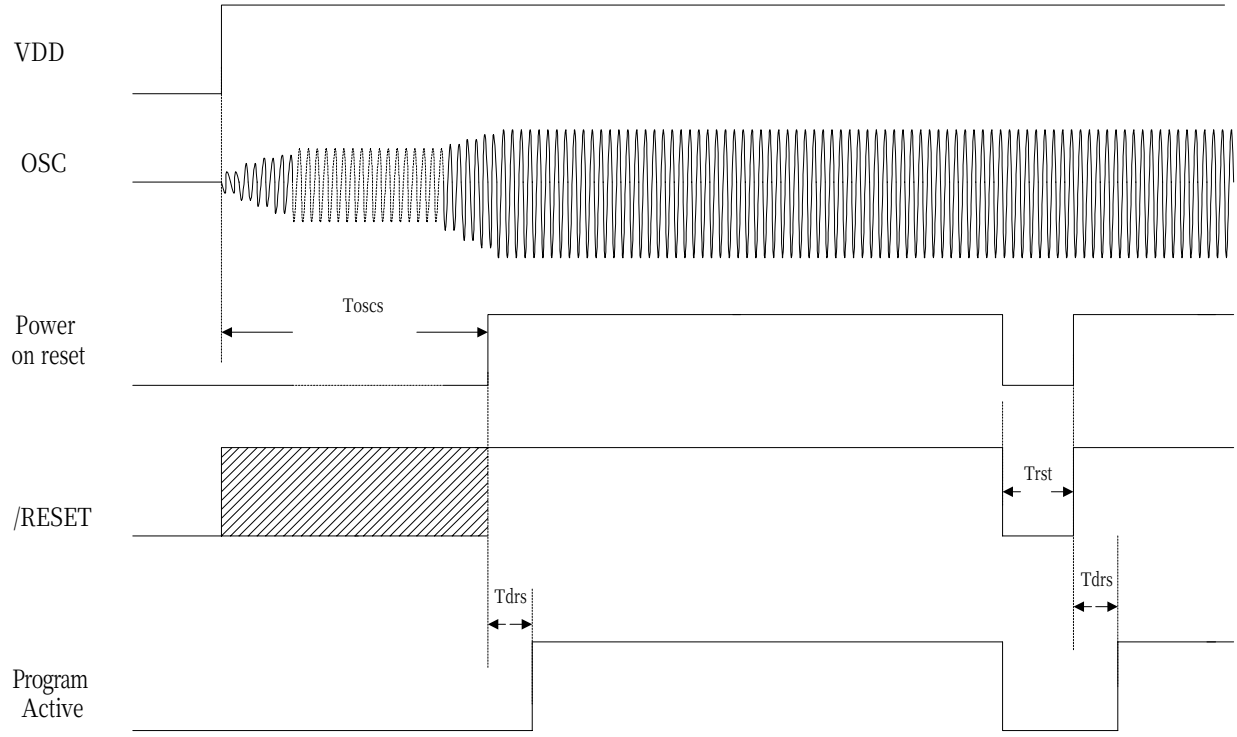
ADC characteristic (VDD = 5V, Ta = +25°C, for internal reference voltage)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Upper bound offset voltage	Vofh			44	52.8	mV
Lower bound offset voltage	Vofl			32	38.4	mV

*These parameters are characterized but not tested.
* About ADC characteristic, please refer to next page.

Timing characteristic (AVDD=VDD=5V,Ta=+25°C)

Description		Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic						
OSC start up	32.768kHz	Toscs	400		1500	ms
	3.579MHz PLL			5	10	us
SPI timing characteristic (CPU clock 3.58MHz and Fsco = 3.58Mhz /2)						
/SS set-up time		Tcss	560			ns
/SS hold time		Tcsh	250			
SCLK high time		Thi	250			ns
SCLK low time		Tlo	250			ns
SCLK rising time		Tr		15	30	ns
SCLK falling time		Tf		15	30	ns
SDI set-up time to the reading edge of SCLK		Tisu	25			ns
SDI hold time to the reading edge of SCLK		Tihd	25			ns
SDO disable time		Tdis			560	ns
Timing characteristic of reset						
The minimum width of reset low pulse		Trst	3			uS
The delay between reset and program start		Tdrs		18		mS



The relative between OSC stable time and power on reset

EM78P5830A operation voltage(X axis → min VDD ; Y axis → main CLK):

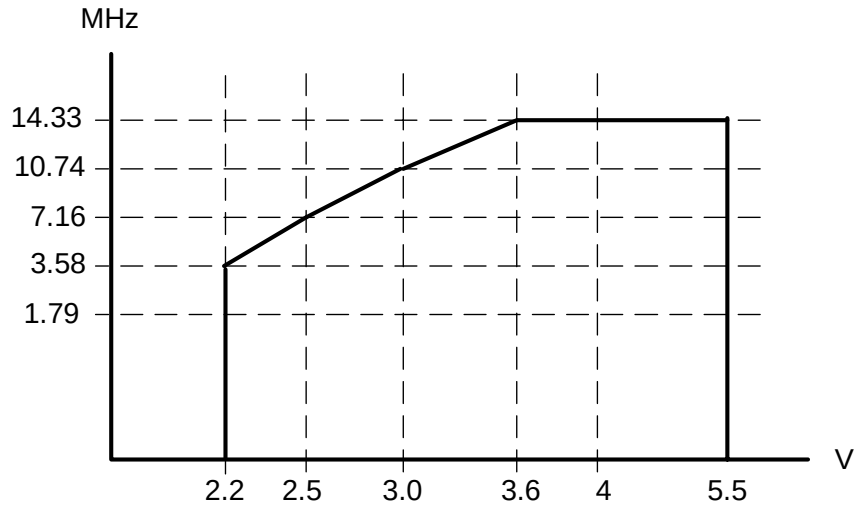


Fig.15 The relative between operating voltage and main CLK

EM785830AA's 10 bit ADC characteristic

EM785830AA build in 10 bit resolution, multi channel ADC function. In ideal, if ADC's reference voltage is 5V, the ADC's LSB will be 5V/1024. But in practical, for some physics or circuit's character, some un-ideal will effect the converter result. As the next figure, offset voltage will reduce AD's converter range. If AD's input voltage less than VOFL, ADC will output 0; in opposition, if input voltage is larger than (VDD-VOFH), ADC will output 1023. That is to say the physics AD converter range will replace by (VDD-VOFH+LSB-VOFL+LSB). If we defined that VRB = VOFL – LSB and VRT = VDD-VOFH+LSB, the physics LSB is:

LSB = (VRT - VRB) / 1024

= ***(VDD – (VOFH+VOFL)) / 1022***

For real operating, please think about the effect of AD's offset voltage. If converter the range of (VRT - VRB), the AD converter's opposite result will be précised.

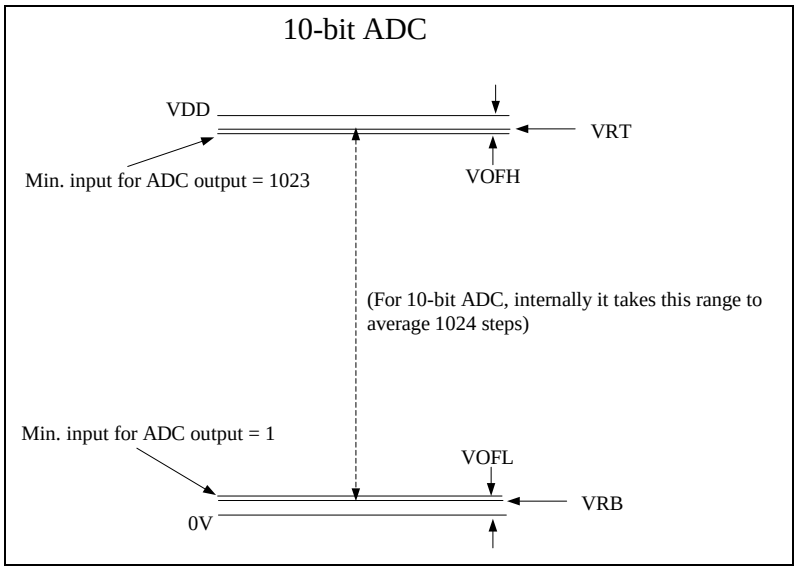
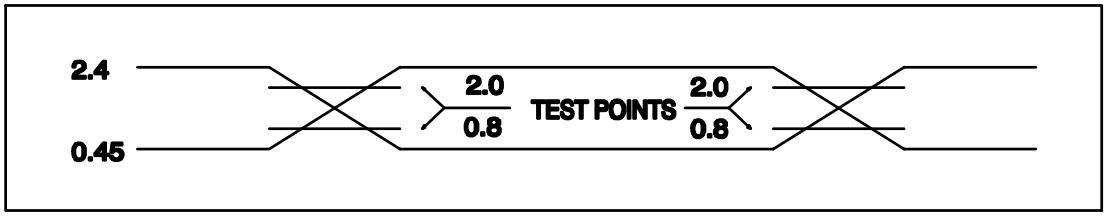


Fig.16 The relative between ADC and offset voltage

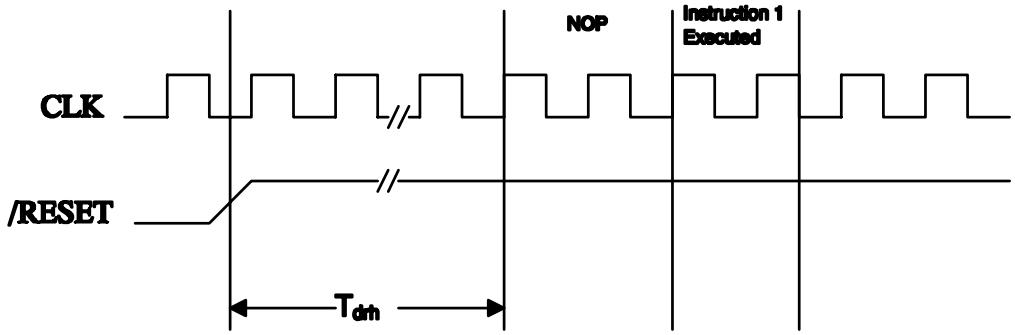
XII. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

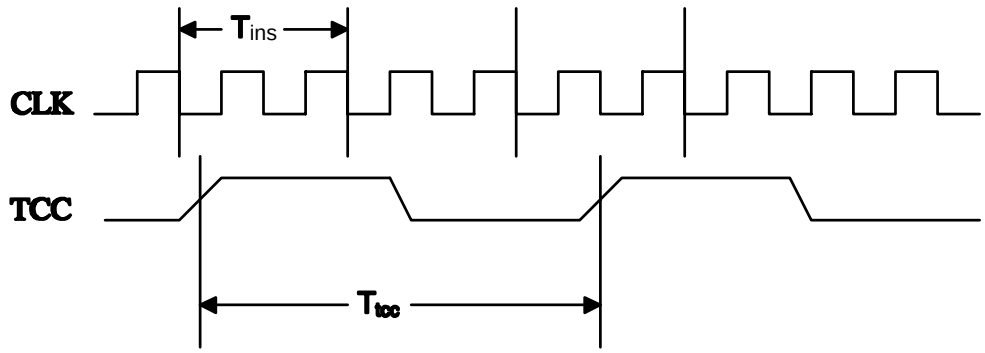


Fig.17 AC timing

Appendix I: Describe of EM78P5830A/AA (only list the difference between mask and OTP)

The EM78P5830A is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. There are 16Kx13 bits Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides security bits and some One time programmable Option bits to protect the OTP memory code from any external access as well as to meet user's options.

This integrated single chip has an on_chip watchdog timer (WDT), program OTP-ROM, data RAM, programmable real time clock/counter, internal interrupt, power down mode, built-in three-wire SPI, dual PWM(Pulse Width Modulation), 4-channel 10-bit A/D converter and tri-state I/O.

Feature

CPU

- Operating voltage : 2.2V~5.5V at main CLK less then 3.58MHz.

Main CLK(Hz)	Under 3.58M	7.16M	10.74M	14.3M
Operating Voltage(min)	2.2	2.5	3	3.6

- 16k x 13 on chip Electrical One Time Programmable Read Only Memory (OTP-ROM)
- 0.5k x 8 on chip data RAM
- Up to 21 bi-directional tri-state I/O ports(4 shared with AD input; 1 shared with external interrupt input)
- 16 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- two 8-bit counters : COUNTER1 and COUNTER2
- On-chip watchdog timer (WDT)
- 99.9% single instruction cycle commands
- Three modes (Main clock can be programmed from 447.829k to 14.3MHz generated by internal PLL)

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- 7 level Normal mode frequency : 447.8K , 895.7K , 1.79M , 3.58M , 7.16M , 10.75M and 14.3MHz.
- Input port interrupt function
- Dual clocks operation (Internal PLL main clock , External 32.768KHz)

SPI

- Serial Peripheral Interface (SPI) : a kind of serial I/O interface
- Interrupt flag available for the read buffer full,
- Programmable baud rates of communication
- Three-wire synchronous communication. (shared with IO)

PWM

- Dual PWM (Pulse Width Modulation) with 10-bit resolution
- Programmable period (or baud rate)
- Programmable duty cycle

ADC

- Operating : 2.5V 5.5V
- 4 channel 10-bit successive approximation A/D converter
- Internal (VDD) or external reference

POR

- 2.0V Power-on voltage detector reset

PACKAGE

28 pin PDIP and SOP package(300 mil)

One time programmable ROM burner pin

OTP PIN NAME	MASK ROM PIN NAME	P.S.
VDD	AVDD	
VPP	/RESET	
DINCK	P65	
ACLK	P64	
PGMB	P63	
OEB	P62	
DATA	P73	
GND	AVSS	

EM78P5830A CODE Option Register

13	12	11	10	9	8	7	6	5	4	3	2	1	0
		0	***0***	***1***						MER			/POT0

Bit 0 (/POT0): program ROM protect option.

If set 1 to the bit, program memory can be access; else if clear this bit , program memory can not be access.

Bit 3(MER) : Memory error recover function

0 ➔ disable memory error recover function

1 ➔ enable memory error recovery function

If user enable memory error recovery function, MCU will improve effect from environment noise**.**

Bit 9: Please set this bit to 1.

Bit 10: Please clear this bit to 0.

Bit 11: Please clear this bit to 0.

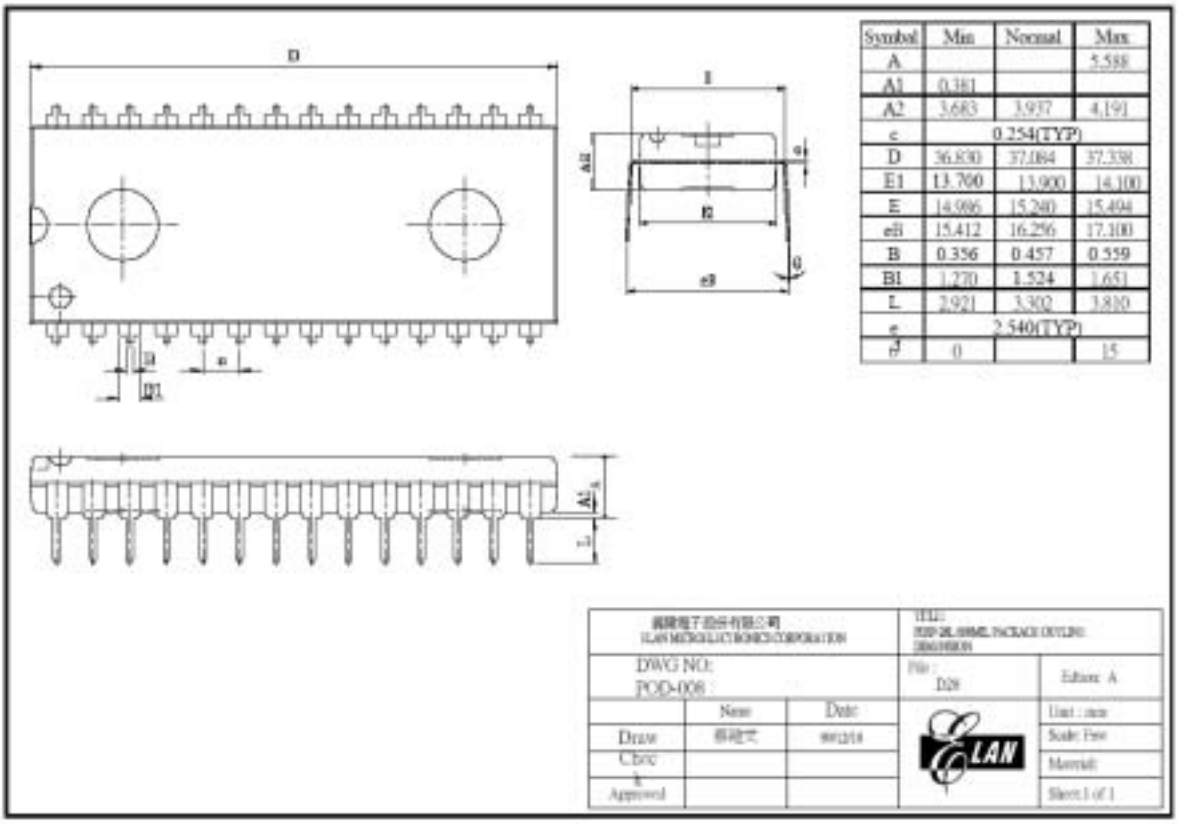
DC Electrical Characteristic

(Ta = 25°C, AVDD=VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output high voltage for PORT62~PORT67	VOH2	IOH = -10mA	2.4			V
Output high voltage for PORT7 ; PORT9	VOH3	IOH = -20mA	2.4			V
Output low voltage for PORT62~PORT67	VOL2	IOH = 10mA			0.4	V
Output low voltage for PORT7 ; PORT9	VOL3	IOH = 20mA			0.4	V

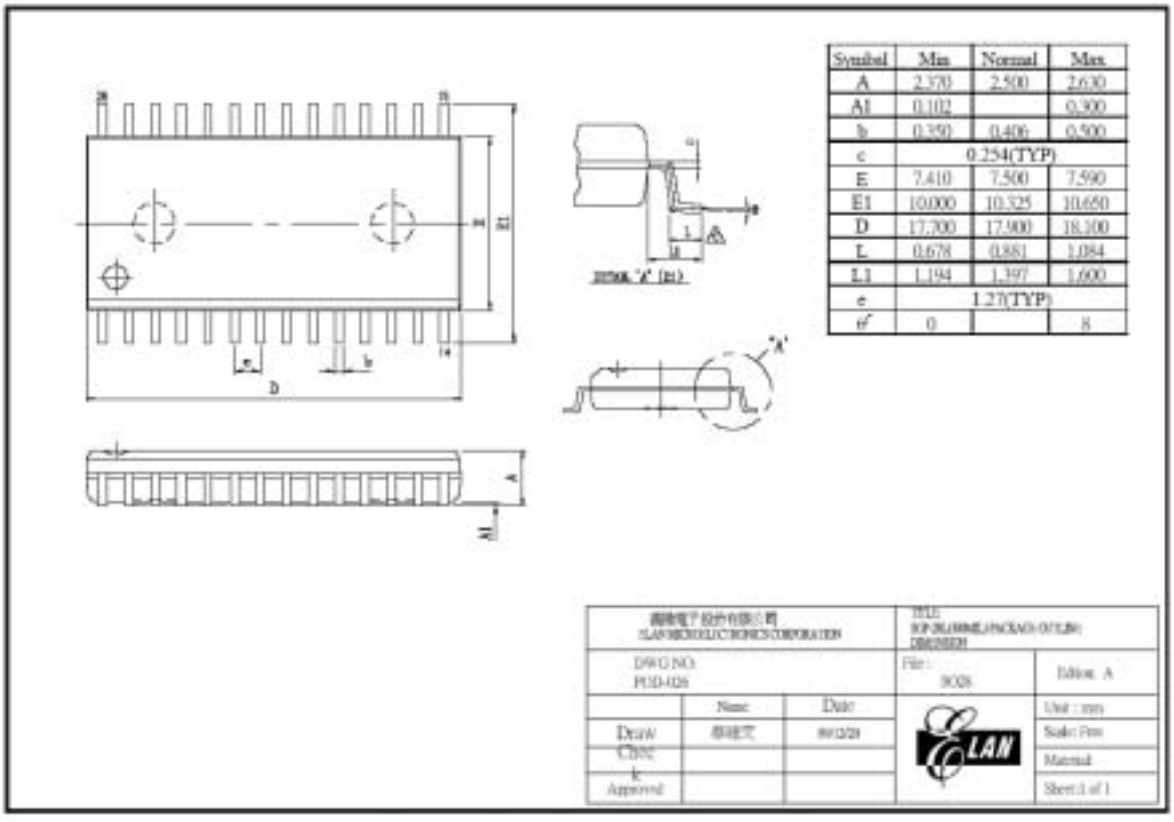
Appendix II: Package spec of EM785830AA, EM78P5830A/AA

EM785830AAP, EM78P5830AP, EM78P5830AAP



Symbol	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	36.830	37.084	37.338
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ°	0		15

EM785830AAM, EM78P5830AM, EM78P5830AAM



Symbol	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ°	0		8